MOTOROLA Semiconductors

MC8507
MC6828

Note: The dual numbering system emphasizes that this device is a bipolar LSI device **and** directly compatible with the M6800 Microprocessor Family. The Priority Interrupt Controller may be ordered by using either part number.

MEGALOGIC

PRIORITY INTERRUPT CONTROLLER

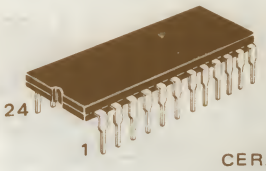
PRIORITY INTERRUPT CONTROLLER

The MC8507/6828 Priority Interrupt Controller (PIC) is used to add prioritized responses to inputs to microprocessor systems. The performance has been optimized for the M6800 system, but will serve to eliminate input polling routines from any processor system.

The MC8507/6828 PIC modifies the ROM address which the processor uses to find the start of the polling or other interrupt service routine. When using the PIC in non-M6800 systems, the address for the service routine must end in . . . 1100x (where x indicates the don't care state of the LSB of the address), and any second byte of the routine address must also end in . . . 1100x.

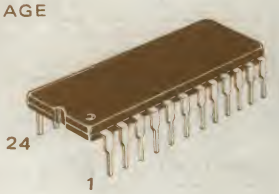
The PIC allows for any added decode time by generating a $\overline{\text{Stretch}}$ signal which can be used to slow the processor clock while fetching interrupt routine starting addresses. The $\overline{\text{Stretch}}$ signal allows the interrupt structure to be designed without concern for faster operation due to improvements in processor speeds.

An interrupt mask prevents any latched interrupt input of lower priority than the mask level from generating an $\overline{\text{IRQ}}$ output.

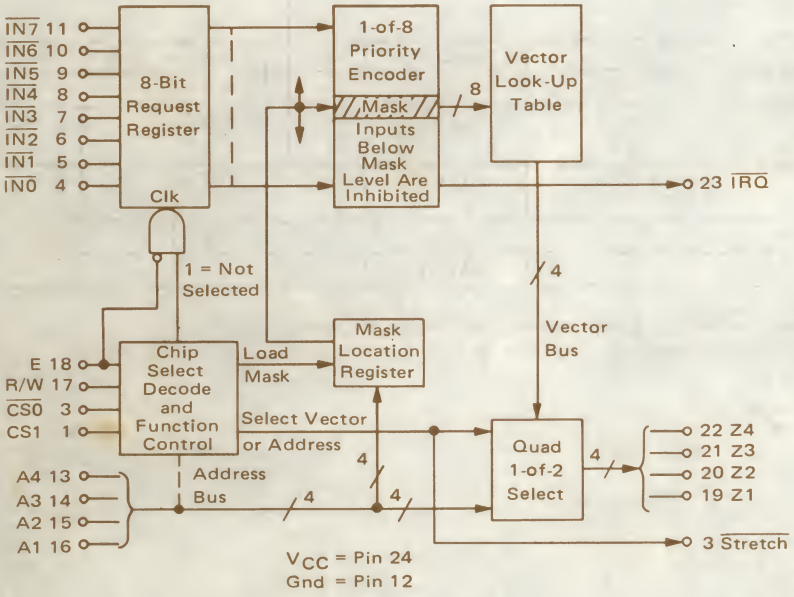


L SUFFIX
CERAMIC PACKAGE
CASE 623

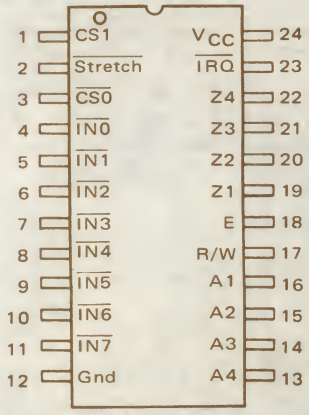
P SUFFIX
PLASTIC PACKAGE
CASE 649



BLOCK DIAGRAM



PIN ASSIGNMENT



MEGALOGIC is a trademark of Motorola Inc.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-1.0 to +5.5	Vdc
Output Voltage	V_{OH}	-0.4 to +7.0	Vdc
Thermal Resistance	θJA	65	°C/W
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, T_A = 0 to 75° unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
Input Forward Current		I_{IL}			μAdc
(V_{IL} = 0, V_{CC} = 5.25 Vdc)	CS1, E		–	-75	
	$\overline{CS0}$, R/W		–	-150	
	A1 thru A4		–	-225	
	$\overline{IN0}$ thru $\overline{IN7}$		–	-1.300	
Input Leakage Current		I_{IH}			μAdc
(V_{IH} = 2.4 Vdc, V_{CC} = 5.25 Vdc)	CS1		–	120	
	$\overline{CS0}$		–	240	
	A1 thru A4		–	360	
	$\overline{IN0}$ thru $\overline{IN7}$		–	-560	
Logic "0" Output Voltage		V_{OL}			Vdc
(I_{OL} = 1.6 mAdc, V_{ILT} = 0.8 Vdc, V_{IHT} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	Z1 thru Z4, $\overline{Stretch}$		–	0.5	
(I_{OL} = 3.2 mAdc, V_{CC} = 4.75 Vdc)	$\overline{IRQ}$ – Open Collector		–	0.5	
Logic "1" Output Voltage		V_{OH}	2.4	–	Vdc
(I_{OH} = -0.3 mAdc, V_{ILT} = 0.8 Vdc, V_{IHT} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	Z1 thru Z4, $\overline{Stretch}$				
Output Leakage Current		I_{CEX}	–	100	μAdc
(V_{CC} = V_{CEX} = 5.25 Vdc)	$\overline{IRQ}$				
Power Supply Drain Current		I_{CC}	–	117	mAdc
(V_{CC} = 5.0 Vdc, All Inputs Open)					

SWITCHING TIMES (V_{CC} = 5.0 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
A_i to Z_i Delay Time (Not Selected)	t_{AZ}	–	50	–	ns
Select* to Z_i Delay Time ($\bar{A}1 \cdot \bar{A}2 \cdot A3 \cdot A4 \cdot \overline{CS0} \cdot CS1$ to Z_i)	t_{CSZ}	–	125	–	ns
Select* to $\overline{Stretch}$ Delay Time ($\bar{A}1 \cdot \bar{A}2 \cdot A3 \cdot A4 \cdot \overline{CS0} \cdot CS1$ to $\overline{Stretch}$)	t_{STR}	–	110	–	ns
Enable to $\overline{IRQ}$ Delay Time, Non-Masked Mode	t_{IRQ}	–	220	–	ns
Enable to $\overline{IRQ}$ Delay Time, Masked Mode	t_{MIRQ}	–	**	–	ns

*Select = ($\bar{A}1 \cdot \bar{A}2 \cdot A3 \cdot A4 \cdot \overline{CS0} \cdot CS1 \cdot R/W$) which corresponds to FFF8 or FFF9 interrupt response in the M6800 system.

**Value depends on mask level and stored priority input. Maximum value occurs with mask level 8 and stored interrupt $\overline{IN0}$. Minimum value occurs with mask level J and stored interrupt $\overline{IN(J-1)}$.

FIGURE 4 – BASIC FUNCTIONAL FLOW CHART

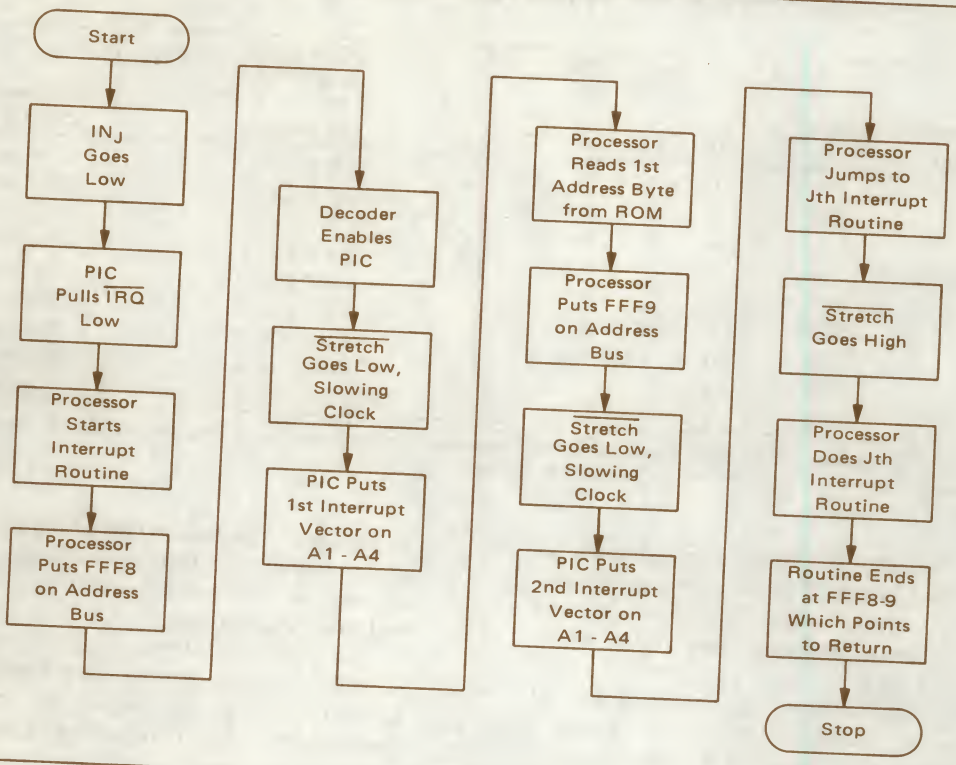
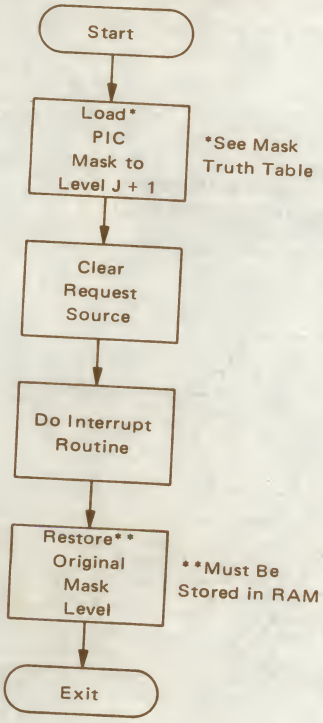


FIGURE 5 – MASK OPERATION

a – MASK FLOW CHART



b – MASK TRUTH TABLE

Mask Register Contents				Response to Priority Inputs 1 = Response to Input, 0 = No Response.							
M4	M3	M2	M1	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
1	1	1	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0
0	1	1	0	1	1	0	0	0	0	0	0
0	1	0	1	1	1	1	0	0	0	0	0
0	1	0	0	1	1	1	1	0	0	0	0
0	0	1	1	1	1	1	1	1	0	0	0
0	0	1	0	1	1	1	1	1	1	0	0
0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	1	1	1

FIGURE 2 – MC8507 TRUTH TABLE FOR M6800 MICROPROCESSOR SYSTEMS

Active Input		Output When Selected Z4	Z3	Z2	Z1	Equivalent to Bits 1-4 of B0, B1 . . . , B15 Hex Address	Address ROM Bytes Contain Address of:
Highest	$\overline{IN7}$	1	0	1	1	F F F 6 or 7	Priority 7 Routine
	$\overline{IN6}$	1	0	1	0	F F F 4 or 5	Priority 6 Routine
	$\overline{IN5}$	1	0	0	1	F F F 2 or 3	Priority 5 Routine
	$\overline{IN4}$	1	0	0	0	F F F 0 or 1	Priority 4 Routine
	$\overline{IN3}$	0	1	1	1	F F E E or F	Priority 3 Routine
	$\overline{IN2}$	0	1	1	0	F F E C or D	Priority 2 Routine
	$\overline{IN1}$	0	1	0	1	F F E A or B	Priority 1 Routine
Lowest	$\overline{IN0}$	0	1	0	0	F F E 8 or 9	Priority 0 Routine
	None	1	1	0	0	F F F 8 or 9	Default Routine*

*Default routine is the response to interrupt requests not generated by a prioritized input. The default routine may contain polling routines or may be an address in a loop for an interrupt driven system.

puts $\overline{IN0}$, $\overline{IN1}$, $\overline{IN2}$, and $\overline{IN3}$ would not generate an interrupt to the MPU system. The input request register is not affected by the mask, and if the mask is cleared (by loading it with zeros) any previously stored inputs will generate an $\overline{IRQ}$ signal.

The chip select and decode circuitry controls all internal functions of the PIC. The selected mode is defined as the logical AND function $\overline{A1} \cdot \overline{A2} \cdot A3 \cdot A4$ $\overline{CS0} \cdot CS1 \cdot R/\overline{W}$. When the device is not in the selected mode the request register clock is enabled and the address inputs A_i pass directly through the data selector to the Z_i outputs. When the MPU responds to interrupt request $\overline{IRQ}$ and the PIC decodes the select address, the request register is inhibited and the data selector places the vector on the Z outputs. The address delay added to the MPU system is shown in Figure 3. This delay may be critical in some systems. A stretch signal, which indicates the selected mode, is provided for use with special MPU clock drivers to stretch the clock cycle when accessing slow ROMs. The $\overline{CS0}$ input has one less gating level than the remainder of the select decode logic. This allows an external NAND gate to be used for the full address decode without any increase in delay times.

The decode logic also controls the loading of the mask location register. This register will be loaded on the falling edge of the enable pulse when enabled by the logical AND function $\overline{CS0} \cdot CS1 \cdot \overline{R/W}$ (note 1). Contrary to normal read/write operations in MPU systems, the "data" written into the mask register are bits A1 thru A4 of the address bus (see Figure 5). This means that in the load mask mode the data on the data bus is a don't care. However in this mode the ROM will also be accessed and both the ROM and MPU will be driving the data bus. Therefore the read/write line should be used as an active high chip select or enable signal for ROM decoding.

Figure 4 show the typical operation flow diagram for the PIC in an M6800 system. The functional timing for this flow is as shown in the first part of the waveforms in Figure 1. The second half of Figure 1 shows the operation of the mask. Interrupts will be stored even if they are masked. When the mask is released the $\overline{IRQ}$ signal will then be generated.

The influence of the mask register on the priority encoder is shown in the truth table of Figure 5. The actual use of the mask register will vary with the system needs and the imaginative software programmer.

Note 1. Since during normal operation of the MPU the address lines and the R/W line can be in an indeterminate state, VMA should be logically ANDed with one of the chip select inputs of the PIC to prevent erroneous writes into the mask register.

FIGURE 3 – HIGH ROM ADDRESS DELAY ADDED TO M6800 SYSTEM

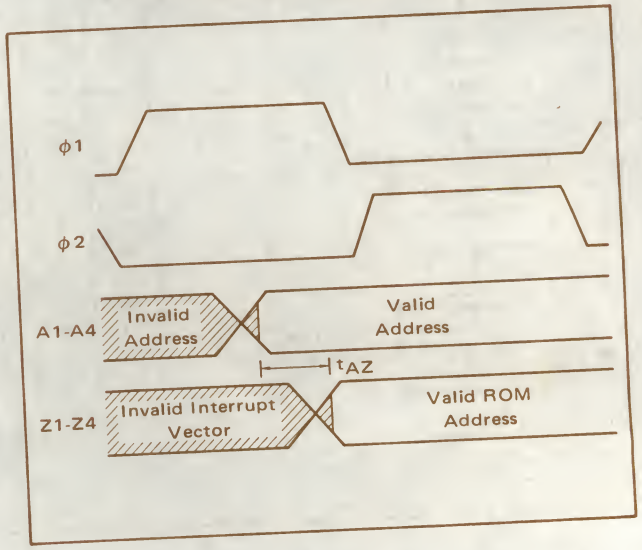
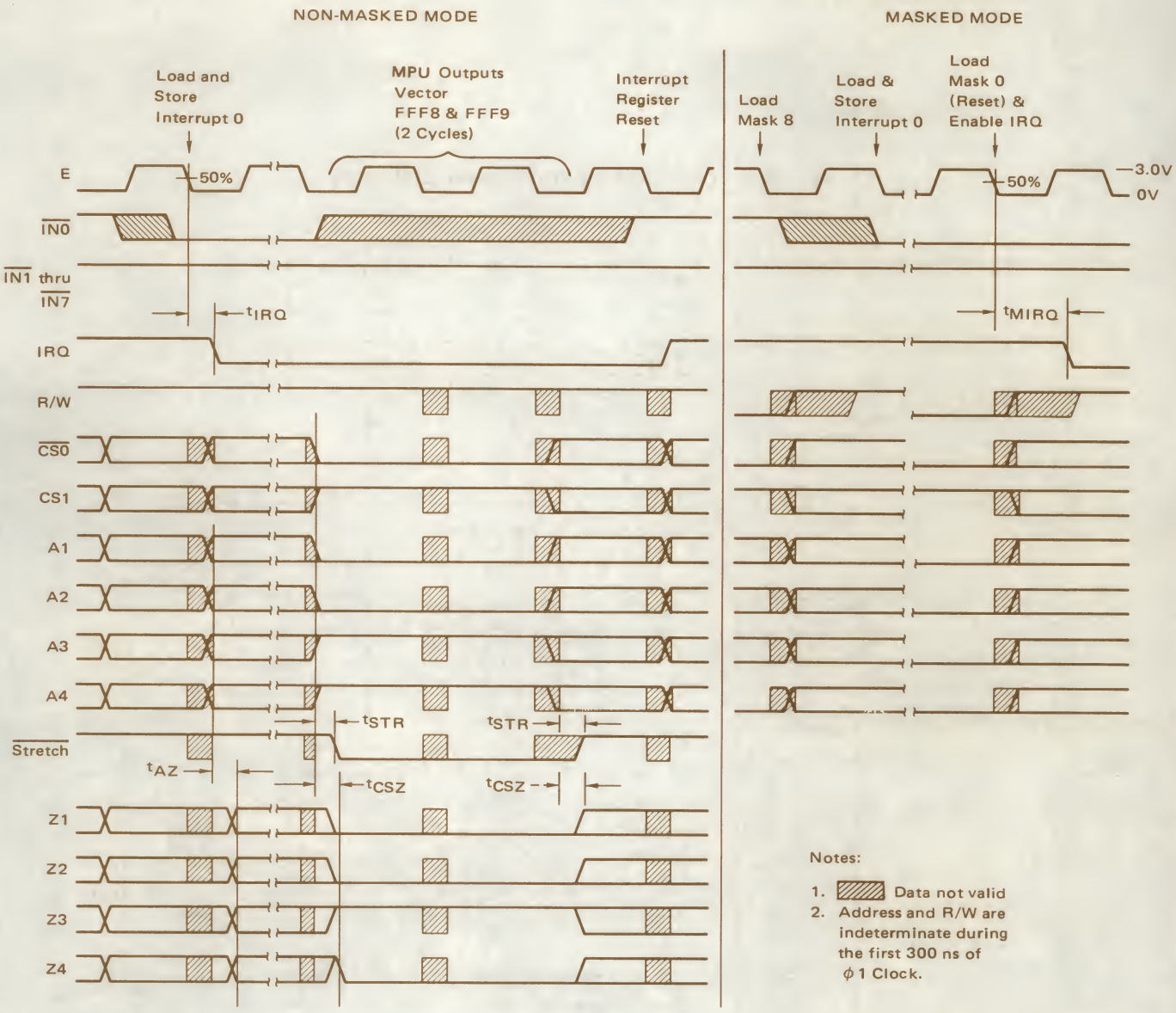


FIGURE 1 – FUNCTIONAL WAVEFORMS



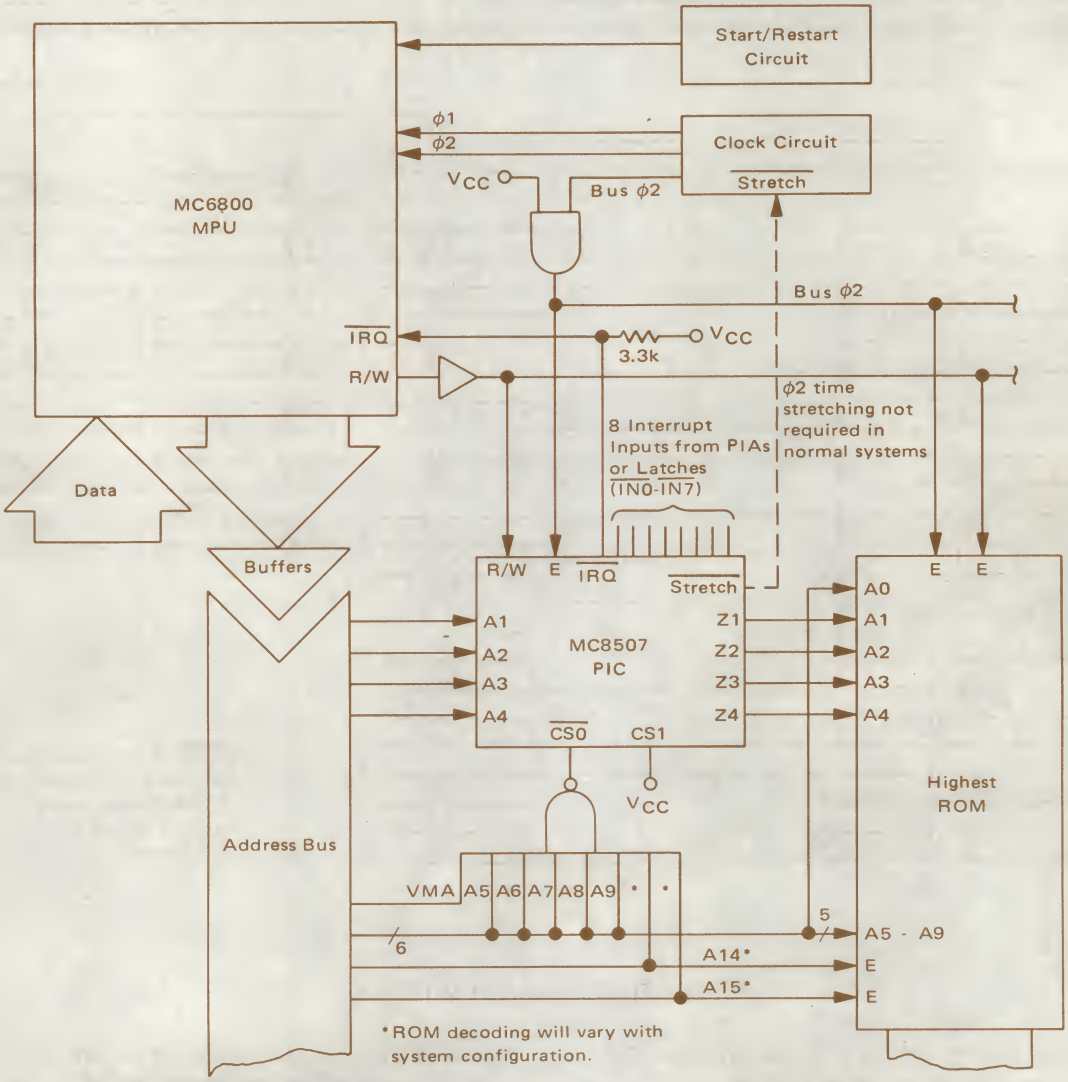
OPERATING CHARACTERISTICS

The primary purpose of the Priority Interrupt Controller (PIC) is to generate a modified address to ROM in response to prioritized inputs. With the PIC, each interrupting device is assigned a unique ROM location which contains the starting address of the appropriate service routine. After the MPU detects and responds to an interrupt the PIC directs the MPU to the proper memory location.

The basic functions of the PIC are shown in the block diagram. The 8-bit request register is an edge clocked D-type register with internal 6 kΩ pullup resistors on the interrupt inputs ($\overline{IN0}$ thru $\overline{IN7}$). Note the inputs are active low. The interrupt register is loaded on the falling edge of the enable when the PIC is not selected.

The 1-of-8 priority encoder enables a vector corresponding to the stored interrupt with the highest priority and places it on the vector input port of a data selector. In addition an interrupt request signal $\overline{IRQ}$ is generated to signal the MPU that an interrupt has been detected. The mask location register overides and inhibits all interrupts with priority below the mask level. The mask can be thought of as a movable partition allowing responses to inputs equal to or greater than the mask value. For example if the stored mask level was 4, in-

FIGURE 6 – TYPICAL M6800 SYSTEM CONFIGURATION



MOTOROLA Semiconductor Products Inc.

Printed in Switzerland 53-C78/3.5